

What is claimed is:

1. A flash memory device comprising:  
a memory array with primary and redundant memory cells; and  
redundant fuse circuitry used to replace the primary memory cells with the  
redundant memory cells, wherein the redundant fuse circuitry stores an error code  
indicating a type of defect.
2. The flash memory device of claim 1 wherein the redundant fuse circuitry  
further stores the addresses of defective primary cells and compares the addresses with  
address requests to replace the primary memory cells with redundant memory cells.
3. The flash memory device of claim 1 further comprising:  
control circuitry to control memory operations to the memory array, wherein the  
control circuitry performs an erase operation algorithm that is specific to an error code in  
the redundant fuse circuitry.
4. The flash memory device of claim 1 wherein the error code indicates a row to  
column short.
5. The flash memory device of claim 1 wherein the error code indicates a row-to-  
row short.
6. The flash memory device of claim 1 wherein the error code indicates an  
isolated defect.
7. The flash memory device of claim 1 wherein the error code comprises two  
bits.
8. A flash memory device comprising:  
at least one register to store an address of a defective element in a primary  
memory array, the register having at least one data bit to store an error code; and

a state machine to execute an algorithm based on the error code stored in the register.

9. The flash memory device of claim 8 wherein the error code indicates a type of defect that is associated with the defective element in the primary memory array.

10. The flash memory device of claim 8 wherein the error code comprises multiple bits.

11. The flash memory device of claim 8 wherein the register includes a bank of either fuses, anti-fuses, or non-volatile cells.

12. A flash memory device comprising:  
a memory array;  
redundant array elements;  
a register for each redundant array element to store an address of a defective element in the memory array, each register further stores an error code;  
a redundant circuit to redirect address requests from the defective element to an associated redundant array element; and  
control circuitry to execute an algorithm based on the error code stored in the register.

13. The flash memory device of claim 12 wherein the redundant element is a redundant row.

14. The flash memory of claim 12 wherein the redundant element is a redundant column.

15. The flash memory device of claim 12 wherein the algorithm controls an erase operation of the memory array.

16. The flash memory of claim 12 wherein the redundant circuit redirects address requests from the at least one defective element to an associated redundant element when an address request matches an address in a register.

17. A flash memory device comprising:  
a memory array having memory cells arranged in columns and rows;  
at least one redundant row coupled to the memory array to replace an associated defective row in the memory array; and  
a register for each redundant row to store the address of the associated defective row, each register further stores an error code, wherein the error code indicates the type of error the redundant row is used to correct.

18. The flash memory device of claim 17 further comprising:  
a redundant circuit to redirect address requests from the defective row in the memory array to the redundant row.

19. The flash memory device of claim 17 further comprising:  
a state machine to control erase operations, the state machine having an algorithm that directs specific erase operations in response to an error code in a register.

20. A flash memory device comprising:  
a memory array having memory cells arranged in columns and rows;  
at least one redundant column mapped to the memory array to replace an associated defective column in the memory array; and  
a register for each redundant column to store the address of the associated defective column, each register having at least one extra bit to store an error code, wherein the error code indicates the type of error in the at least one defective column.

21. The flash memory device of claim 20 further comprising:  
a redundant circuit to redirect address requests from the defective column in the memory array to the associated redundant column.

22. The flash memory device of claim 20 further comprising:  
control circuitry to control erase operations, wherein the control circuitry directs specific erase operations in response to the type of error code stored in the register.

23. The flash memory device of claim 20 wherein the error code comprises two bits.

24. A flash memory device comprising:  
a memory array having memory cells arranged in columns and rows;  
at least one redundant row to replace an associated defective row in the memory array;  
a register for each redundant row to store the address of an associated defective row, each register further having at least one bit to store an error code, wherein the error code indicates the type of defect in the associated defective row;  
a redundant circuit to compare address requests to the addresses in the registers, wherein the redundant circuit directs address requests matching addresses in the registers to the associated redundant row instead of the defective row in the memory array; and  
control circuitry to execute an erase operation algorithm based on the error code stored in each register.

25. The flash memory system of claim 24 wherein the erase operation algorithm disables the redundant circuit during a pre-programming cycle and a soft programming cycle of an erase operation when the error code indicates a row to row short.

26. The flash memory system of claim 25 wherein the control circuitry simultaneously programs the rows shorted together during the pre-programming cycle.

27. The flash memory system of claim 25 wherein the control circuitry simultaneously applies a soft program pulse to the rows shorted together during the soft programming cycle if an over erased cell is detected in one of the rows.

28. A flash memory device comprising:  
a memory array having memory cells arranged in columns and rows;  
at least one redundant row to replace an associated defective row in the memory array;  
at least one redundant column to replace an associated defective column in the memory array; and  
a register for each redundant row and each redundant column to store the addresses of associated defective rows and columns, each register having at least one bit to store an error code, wherein the error code indicates the type of defect the redundant row or column is used to correct.

29. The flash memory device of claim 28 further comprising:  
a first redundant circuit to redirect address requests from the defective column in the memory array to the associated redundant column; and  
a second redundant circuit to redirect address requests from the defective row in the memory array to the associated redundant row.

30. The flash memory device of claim 28 further comprising:  
a state machine to control erase operations in response to the error code in a register.

31. A flash memory system comprising:  
a processor to provide data;  
a memory array to store data from the processor;  
at least one redundant element to replace an associated defective element in the memory array;  
a register for each redundant element to store the address of an associated defective element, each register having at least one extra bit to store an error code, wherein the error code indicates the type of defect in the defective element;  
a redundant circuit to compare address requests to the addresses in the registers, wherein the redundant circuit directs address requests matching addresses in the registers

to the associated redundant element instead of the defective element in the memory array;  
and

control circuitry to execute an erase operation algorithm based on the error code stored in a register.

32. The flash memory system of claim 31 wherein the defective element is a defective row and the redundant element is a redundant row.

33. The flash memory system of claim 31 wherein the defective element is a defective column and the redundant element is a redundant column.

34. A flash memory system comprising:  
a processor to provide data;  
a memory array to store data from the processor, the memory array having memory cells arranged in columns and rows;  
at least one redundant row to replace an associated defective row in the memory array;  
at least one redundant column to replace an associated defective column in the memory array;  
a register for each redundant row and each redundant column to store the address of each associated defective row and each associated defective column, each register having at least extra one bit to store an error code, wherein the error code indicates the type of defect in the respective defective row or column;  
a redundant circuit to compare address requests to the addresses in the registers, wherein the redundant circuit directs address requests matching addresses in the registers to the associated redundant row or column instead of the defective row or column in the memory array; and  
a state machine to execute an erase operation algorithm based on the error code stored in each register.

35. The flash memory system of claim 34 wherein the redundant circuit comprises:

a first redundant circuit to compare address requests to defective columns in the memory array; and

a second redundant circuit to compare address requests to defective rows in the memory array.

36. The flash memory system of claim 34 wherein the erase operation algorithm disables the redundant circuit during the pre-programming and soft programming cycles of an erase operation when the error code indicates a row to column short.

37. The flash memory system of claim 34 wherein the erase operation algorithm disables the redundant circuit during the pre-programming and soft programming cycles of an erase operation when the error code indicates a row to row short.

38. The flash memory system of claim 37 wherein the state machine simultaneously programs the rows shorted together during the pre-programming cycle.

39. The flash memory system of claim 37 wherein the state machine simultaneously applies a soft program pulse to the rows shorted together during the soft programming cycle if an over-erased cell is detected in a column coupled to the rows.

40. A method of operating a flash memory comprising:  
initiating an erase operation on a memory array having redundant elements;  
matching a requested address with an address of a defective element stored in a register associated with a redundant element;  
reading an error code stored in the register; and  
executing an erase operation algorithm based on the error code.

41. The method of claim 40 wherein the redundant element includes a pair of redundant rows and the error code indicates a row-to-row short, a pre-programming cycle of the erase operation further comprises:

- pre-programming the redundant rows;
- pre-programming each row in a primary array until a row address matches a redundant row address;
- disabling a redundant circuit that points the row address request from the defective row in the primary array to the redundant row;
- activating first and second rows in the primary array, wherein the first and second rows are shorted together;
- pre-programming the first and second rows simultaneously; and
- pre-programming each row in the primary array following the first and second rows.

42. The method of claim 40 wherein the redundant element includes a pair of redundant rows and the error code indicates a row-to-row short, a  $V_t$  (threshold voltage) tightening cycle of an erase operation further comprises:

- monitoring each column of the memory array to determine if a current level in the column is above a threshold level that would indicate an over-erased cell is coupled to the column;
- when current is found in a column above the threshold value, applying a program pulse to redundant rows coupled to the column;
- verifying if the current level is still above the threshold value;
- when current level is still above the threshold value, applying the program pulse to each row in a primary array coupled to the column until a current above the threshold level can no longer be detected in the column; and
- when encountering first and second rows, wherein the first and second rows are shorted together, applying the program pulse to the first and second rows simultaneously.

43. The method of claim 40 wherein the redundant element includes a redundant row and a redundant column and the error code indicates a row to column short, a pre-programming cycle of the erase operation further comprises:

- pre-programming the redundant rows and columns;

- pre-programming each row and column in a primary array until a row or column address matches a redundant row or column address;

- disabling a redundant circuit that points the row or column address request from the shorted row and column in the primary array to the redundant row or column;

- pre-programming the shorted row and column; and

- pre-programming the remaining rows.

44. The method of claim 40 wherein the redundant element includes a redundant row and redundant column and the error code indicates a row to column short, a soft program cycle of an erase operation further comprises:

- monitoring each column of the memory array to determine if a current level in the column is above a threshold level that would indicate an over-erased cell is coupled to the column;

- when a current level in a column is above the threshold level, verifying if the column address matches an address in a register associated with a redundant column;

- when the column address matches the redundant column address, disabling the redundant circuit;

- applying a  $V_t$  tightening pulse to the redundant rows coupled to the column;

- verifying if the current level in the column is still above the threshold level;

- when the current level in the column is still above the threshold level, applying a  $V_t$  tightening pulse to the rows in a primary array until the current level in the column is below threshold level or a row address matches an address in a register associated with a redundant row;

- when the row address matches the address in the register, disabling a redundant circuit that points the row address request from the defective row in the primary array to the redundant row, applying a  $V_t$  tightening pulse to the defective row in the primary array;

verifying if a current level in the column is still above the threshold level; and  
when a current level in the column is above the threshold level, applying a soft pulse to the cells in the remaining rows until the current can no longer be detected.

45. A method of performing a pre-program cycle of an erase operation on a flash memory having a row-to-row short in the primary array and a pair of redundant rows to replace the rows shorted together comprising:

pre-programming the redundant rows;  
setting the row address to the first address of the primary array;  
pre-programming each row in the primary array incrementally until a row address matches a redundant row address;  
reading an error code that indicates a row-to-row short;  
disabling a redundant circuit that redirects address requests from the shorted rows to the redundant rows;  
activating the shorted rows together;  
pre-programming the shorted rows simultaneously;  
incrementing the row address to skip over the following shorted row; and  
pre-programming the remaining rows in the primary array.

46. The method of claim 45 wherein a row address of a first shorted row is row S and a row address of a following shorted row is row S+1, further wherein an address counter increments a row address to a row S+2 after row S and row S+1 are pre-programmed.

47. A method of performing a heal cycle of an erase operation on a flash memory having a row to row short in the primary array and a pair of redundant rows to replace the rows shorted together comprising;

reading an error code that indicates a row-to-row short;  
setting column address to beginning of primary array;  
monitoring each column incrementally for a current level above a threshold level that would indicate an over-erased cell is coupled to the column;

when a current level above the threshold level is detected in a column, applying a soft program pulse to the redundant rows coupled to the column;

verifying if the current level in the column is still above the threshold level;

when a current level is still above the threshold level, applying a soft program pulse to the rows in the primary array incrementally until the current level in the column is below the threshold level; and

when encountering first and second rows, wherein the first and second rows are shorted together, applying the soft program pulses to the first and second rows simultaneously.

48. The method of claim 47 wherein a row address of the first row in the primary array is row S and a row address of the second row is row S+1, further wherein an address counter increments a row address to a row S+2 after the soft program pulses are applied simultaneously to row S and row S+1.

49. A method of operating a flash memory comprising:  
storing an address of a redundant element in a register;  
storing an error code in the register that corresponds to the type of error the redundant element is used to correct;  
reading the error code; and  
performing an erase operation based on the error code.

50. The method of claim 49 wherein performing an erase operation further comprises:

performing a pre-program cycle;  
performing an erase cycle; and  
performing a soft program cycle.

51. The method of claim 49 wherein the redundant element is a redundant row.

52. The method of claim 49 wherein the redundant element is a redundant column.

53. A method of manufacturing a flash memory comprising:  
testing a memory array for defective elements;  
adding redundant elements to selectively replace the defective elements;  
mapping redundant elements to the memory array;  
storing addresses of redundant elements in associated registers; and  
storing an error code in each register that indicates the type of defect the redundant element is being used to correct.

54. The method of claim 53 wherein a state machine uses the error code to execute an erase operation algorithm to specifically deal with the defective elements in the memory array during an erase operation.

55. A method of manufacturing a flash memory comprising:  
identifying a defective primary element; and  
programming a redundant fuse circuit, wherein the redundant fuse circuit stores a defective code.

56. The method of claim 55 wherein the error code indicates a type of defect in the defective primary element.